AM386SC300

Élan ™ Rev A to Rev B

Change Document

Revision 1.03

ADVANCED MICRO DEVICES
MOBILE COMPUTERS PRODUCT DIVISION

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ÉLAN AM386SC300 REV B OVERVIEW

Élan Am386SC300 Rev B device is a second generation Élan initiative which is hardware backwards compatible with the Élan Am386SC300 Rev A device except for three minor hardware issues which, if incorporated correctly, will allow a Rev A or Rev B Élan to be installed in the same PCB assembly.

Élan Rev B is an Integrated Processor (IP) targeted at the high performance Palmtop, Personal Organizer, and low end sub-notebook portable markets. Functionally, the Élan Rev B is a PC/AT compatible computer on a chip whose goal is to provide the customer with a high performance, low power system solution, providing state of the art power management in a smaller physical foot print than the competition.

The purpose of this document is to provide a high level description of changes to the features and functionality of the Élan Integrated Processor arising from the introduction of the Élan Rev B. Changes to the functionality and programmability of each block are detailed as well as the system level configurability and interfaces.

This document covers only changes. The Data Sheet and Programmer's Reference Guide for either Am386SC300 device, Rev A or Rev B, should be consulted for general information.

Product Features

ENHANCED AM386SXLV(TM) CPU CORE

- **33 MHZ CPU NOW SUPPORTED**

INTEGRATED MEMORY CONTROLLER

- Zero wait-state access with 70ns, 3.3V, Page Mode DRAM's @ 33MHz
- Support for 1Mx16 asymmetrical DRAM
- 512KB x 8 DRAMs (2 Mbyte Total Memory) Enhanced Page Mode supported
- Self Refresh DRAM support
- Refresh Disable in PMU Off mode

INTEGRATED POWER MANAGEMENT FUNCTIONS

- Micro Power Mode Added allowing internal RTC to remain powered while all external peripherals are powered off and no external buffering is required.
- Low Power Consumption.

Mode	Typical 25 Mhz mW	Typical 33 Mhz mW
Full On	464	585
Doze	47	59
Suspend/ Micro Power	0.05	0.05

Notes: Values given for Suspend/Micro Power mode do not take into account the optional VMEM power plane.
All numbers given for 33 Mhz operation and Suspend/Micro Power mode are projected values

INTEGRATED KEYBOARD FEATURES

- PS/2 Compatible Port 92 Fast Reset and A20 Control
- XT Keyboard Support

FUNCTIONAL CHANGE DESCRIPTION

The Élan Rev B Am386SC300 is a follow-on to the Élan. The Am386SC300 device is intended to provide a more cost effective system solution with some feature enhancements. Unless otherwise specified, the Élan Rev B Am386SC300 functions are 100% compatible with the original Élan.

I/O Changes

This section documents the changes to the **Élan Rev B Am386SC300** I/Os.

Programmable drive strengths.

In order to allow more flexibility in driving variable loads, programmable drive strength output buffers have been added to the signals listed below. These signals have been grouped to allow different drive strengths to be programmed through the three control fields of Configuration Register, Index B9H, bits 1:0, 3:2, 5:4, for each of the different signal groups. Refer to section 2.7.8 for a complete description of this register.

Control #1, Index B9H, [1:0]
RAS1#, RAS0#
Control #2, Index B9H, [3:2]
MA10-MA0/SA23-SA13, MWE#
Control #3, Index B9H, [5:4]
D15- D0

Control Bits	Drive Strength
0 0	E
0 1	C
1 0	D
1 1	tri - state

Table 1. I/O Drive Type Description

T_{CASE} = 125° C, VOL_{TTL} = 0.4 volts, VOH_{TTL} = 2.4 volts

DRIVE TYPE	VCC IO (volts)	IOL_{TTL} (mA)	IOH_{TTL} (mA)*
A	3.0	2.6	-3.5
	4.5	3.7	-13.9
B	3.0	5.2	-5.2
	4.5	7.3	-20.7
C	3.0	7.7	-8.6
	4.5	10.8	-34.2
D	3.0	7.7	-10.3
	4.5	10.8	-40.8
E	3.0	10.2	-13.6
	4.5	14.1	-53.9

*Current out of pin is given as a negative value.

Support for 1Mx16 asymmetrical Drams

The SA12 pin has been modified to function as MA11 when 16M bit (1Mx16) asymmetrical DRAMs are used. The SA12 (MA11) output is not a programmable output due to its physical location, but is increased to an "E" size output. Details of this feature are explained in the Memory Controller section.

Because of this change, a new signal has to be used to provide the local address bus signal A12 when in local bus mode. Therefore, in Élan Rev B, pin #145 becomes the signal LVDD# (A12/BALE) to provide A12 in local bus mode. . Refer to section 2.7.2 for a complete description of this register.

Schmidt Trigger Inputs

The RESUME, BL4, BL3, BS2, and BL1 pins of the Élan Rev A are not Schmidt-trigger inputs. This has been corrected in the Élan Rev B design. Table 2 lists all of the Schmidt-trigger inputs for the Élan Am386SC300 Rev B:

Table 2. Élan Rev B Schmidt Trigger Inputs

Pin #	Name	Comments
45	SYSCLK (XTCLK)	(New for **Rev B**)
75	8042CS# (XTDAT)	(New for **Rev B**)
101	ACIN	(New for **Rev B**)
103	SUS/RES	(New for **Rev B**)
106	BL1	(New for **Rev B**)
107	BL2	(New for **Rev B**)
108	BL3	(New for **Rev B**)
109	BL4	(New for **Rev B**)
141	RESIN#	(Existing **Rev A** feature)
192	IOCHRDY	(Existing **Rev A** feature)
110	CD_A#	(Existing **Rev A** feature)
113	BVD2_A	(Existing **Rev A** feature)
114	BVD1_A	(Existing **Rev A** feature)
116	CD_B#	(Existing **Rev A** feature)
119	BVD2_B	(Existing **Rev A** feature)
120	BVD1_B	(Existing **Rev A** feature)

Internal Pull-Ups

The internal pull-up on pin #80, AFDT#, present on Élan Rev A has been removed in Rev B.

Parallel Port Pin Redefinition

The parallel port signals in the Élan Rev B may be re-assigned to provide other functions. Parallel port pin functionality is controlled through the Register, Index BAH, bits 3:4 as follows:

- Bit 4 is used to enable the PCMCIA OE (output enable) PCMCOE# and WR (write) PCMCWE# signals.
- Bit 3 is used to enable the 14.336MHz clock output.

Table 3 describes the new pin functions:

Table 3. Parallel Port Signal Redefinition

Pin #	Parallel Port Signal Name	New Function
80	AFDT#	14MHz clock
84	SLCTIN#	PCMCIA OE#
89	INIT#	PCMCIA WR#

Refer to sections 2.7.9, 5.1, and 5.2 for more details.

8042CS and SYSCLK Alternate Functionality

In Élan Rev B, I/O is affected by a new functionality for pins 8042CS# and SYSCLK. A programmable option that is enabled by setting bit 3 of the Miscellaneous Control Register 3, Index ADH allows the pins to become tristated, so that they may be used as inputs. SYSCLK becomes the KB clock input, while 8042CS# becomes the KB data input for the KB Data Shift Register at port 060H. For more details, see sections 2.6 and 2.7.1 of this document.

Memory Controller

This section documents the changes that have been made in the Élan Am386SC300 Rev B Memory Controller.

Non-Volatile Memory Accesses

The Élan supports two ROM chip selects, ROMCS# and DOSCS#. The ROMCS# chip select is typically used to access the BIOS ROM, and the DOSCS# chip select is used to access an application ROM containing ROMDOS or some other non-volatile memory space. To allow improved ROM performance, and to reduce the access times to the ROM devices, the changes discussed in the following paragraphs have been made to the Élan Rev B.

ROM Chip Select Command Gating

The DOSCS# and ROMCS# chip select outputs in the Élan Rev A are internally gated with the memory read command (MEMR#) or the memory write command (MEMW#). In the Élan Rev B, the following Configuration (Index) Register bits may be used to disable the command gating, and allow the DOSCS# and ROMCS# to be available as address decodes only.

Index B3H, Bit 2 enables the ROMCS# as an address decode.
0 = disabled (default)
1 = enabled

Index B8H, Bit 4 enables the DOSCS# as an address decode.
0 = disabled (default)
1 = enabled

Note: When the CPU clock is stopped, the ROMCS# and DOSCS# chip selects will be forced high**.**

Linear ROM Address Decode

In the Élan Rev A, the DOSCS# ROM may be accessed only by using the MMS. In Rev B, DOSCS# ROM can be accessed from linear address decodes, rather than using the MMS map. If bits 3-0 of Configuration Register, Index B8H are written to values other than logic zeros, then the DOSCS# is decoded from a linear address that corresponds to the value written. If bits 3-0 of Register Index B8H, are cleared (default), then the MMS mapping must be used to access DOS ROM, as shown in Table 4.

Table 4. Linear ROM Address Decode

Index B8H, 3 2 1 0	DOS ROM Linear Address Range	DOS ROM Size
0 0 0 0	disabled, use MMS	N/A, use MMS
0 0 0 1	F00000H - FEFFFFH	~ 1 MB
0 0 1 0	E00000H - FEFFFFH	~ 2 MB
0 0 1 1	D00000H - FEFFFFH	~ 3 MB
0 1 0 0	C00000H - FEFFFFH	~ 4 MB
0 1 0 1	B00000H - FEFFFFH	~ 5 MB
0 1 1 0	A00000H - FEFFFFH	~ 6 MB
0 1 1 1	900000H - FEFFFFH	~ 7 MB
1 0 0 0	800000H - FEFFFFH	~ 8 MB
1 0 0 1	700000H - FEFFFFH	~ 9 MB
1 0 1 0	600000H - FEFFFFH	~ 10 MB
1 0 1 1	500000H - FEFFFFH	~ 11 MB
1 1 0 0	400000H - FEFFFFH	~ 12 MB
1 1 0 1	300000H - FEFFFFH	~ 13 MB
1 1 1 0	200000H - FEFFFFH	~ 14 MB
1 1 1 1	100000H - FEFFFFH	~ 15 MB

The mapping for the ROMCS# will not change. As shown in the preceding table, the DOS ROM size is actually 64KB less than the value listed to avoid overlapping with the ROMCS# decode at FF0000H - FFFFFFH.

High Speed Clock ROM Cycles

To improve the ROM access times in the Élan Am386SC300 Rev B, accesses using the ROMCS# or DOSCS# chip selects may run at the high-speed CPUCLK rate rather than the Low Speed CPU clock rate.

ROMCS#

The High Speed CPUCLK rate is enabled for ROMCS# and unique wait-state controls for each ROM chip select may be programmed through Configuration Register Index B3H.

Index B3H, Bit 6 enables ROMCS# ROM accesses to run at the high-speed CPUCLK rate.
0 = disabled (default)
1 = enabled

Index B3H, Bits [5,4]:

Bits 5 4	Wait States
0 0	4
0 1	3
1 0	2
1 1	1

When the ROMCS# accesses are enabled to run at high speed, Index B3H, bits 4 and 5 control the number of wait states for these cycles as shown in the table above. Note that if the Élan is in its maximum ISA bus mode, the BALE output will not be generated for high speed ROMCS# cycles.

DOSCS#

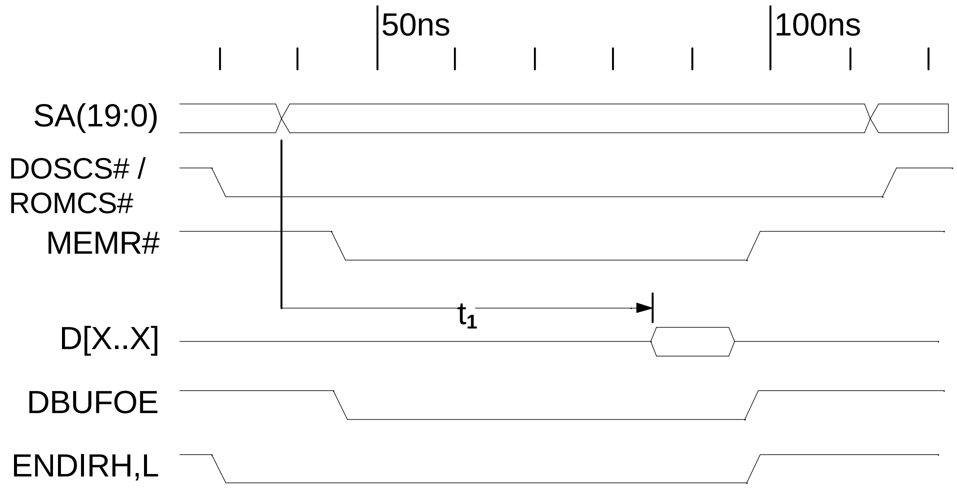
The CPUCLK rate is enabled for DOSCS# and unique wait-state controls for each ROM chip select may be programmed through Configuration Register Index B8H.

Index B8H, Bit 7 enables DOSCS# ROM accesses to run at the high-speed CPUCLK rate.
0 = disabled (default)
1 = enabled

Index B8H, Bits [6,5]:

Bits 6 5	WaitStates
0 0	4
0 1	3
1 0	2
1 1	1

When the DOSCS# ROM accesses are enabled to run at high speed, Index B8H, bits 5 and 6 control the number of wait states for these cycles as shown in the table above. Note that if the Élan is in its maximum ISA bus mode, the BALE output will not be generated for high speed ROMCS# cycles. The time line on the timing diagram shown in Figure 1 is for 33 MHz, 1 wait state cycle where data is strobed into Elan at t = 90ns.



Notes: ELAN Rev. B 33mhz
ROM Cycles using Fast Clock
DOSCS#/ROMCS# generated using address decode only

Figure 1. High Speed Clock Timing

Table 5. SA Stable To Data Valid

WAIT STATES	t_1 (ns)	Notes
1	45	(Preliminary)
2	75	(Preliminary)
3	105	(Preliminary)
4	135	(Preliminary)

Notes: All above numbers allow 5ns Data setup.

Asymmetric 16 Megabit DRAM

Asymmetric 16M bit DRAMS (1M x 16 bit) that RAS 12 address lines and CAS 8 address lines are supported in the Élan Rev B as follows:

- MA11 (SA12) has been added.
- In local bus mode, LVDD/BALE becomes local bus address bit 12.

Refer to sections 2.7.2 and 4.2 for more details.

Self-Refresh DRAMs.

Self-refreshing DRAMS are supported in the Élan Rev B as follows:

- Bit 3 of Register Index B3H enables self-refresh mode when the PMU changes to a mode that causes the CPU clock to stop.
  1 = enabled, 0 (default) = disabled.
- Upon exiting the Stop clock mode, the system logic forces one CAS# before RAS# refresh cycle before the normal CAS# before RAS# refresh logic takes control.
- If a complete burst row refresh is required by the DRAM, Elan will not directly support self-refresh.

33MHz Operation

Improved Élan Rev B timing paths allow operation with 3.3V, 70ns DRAMs at 33MHz.

512Kx8 DRAM, 2M Total System Memory, Enhanced Page Mode Support

The Élan Rev B DRAM provides for enhanced page mode operation with a 2 M byte total memory using two banks. See Table 6 for details.

Table 6. Address Relationships in Enhanced Page Mode When Using 512Kx8 DRAMs

Index 66H	DRAM			DRAM Address											
Bit 4 3 2	Size	Bank 0	Bank 1	RAS CAS	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
0 1 0	2M	1M	1M	RAS CAS	- -	A19 -	A18 A9	A17 A8	A16 A7	A15 A6	A14 A5	A13 A4	A12 A3	A11 A2	A20 A1

80ns DRAM Support

Élan Rev B has been modified to support 80ns DRAM refresh timing requirements. This required that the RAS# pulse width low be extended for CAS# before RAS# refresh cycles during refresh cycles when the CPU clock is stopped for the Rev B part to satisfy the 80nS DRAM RAS# active requirement.

Power Management

This section documents the changes that have been made to the Élan Am386SC300 Rev B Power Management Unit.

Disabling Refresh

Am386SC00 now allows the disabling of Refresh in the PMU Off mode. Setting Configuration Register, Index B9H, bit 7 will cause the RAS and CAS outputs to be driven low when the PMU is in OFF Mode. The system logic should power off the DRAM in this mode, or the low true RAS and CAS outputs may keep the ROW buffers enabled, thus drawing additional power from the DRAM devices.

Note: DRAM memory content is not valid when exiting from Off mode when the disable refresh feature is being used.

Qualifying BL1

The BL1 pin is qualified with ACIN in the Élan Rev B so that it may be used to force the CPU clock to Low Speed only when an external A.C. supply is not present.

Suspend Output Pin States

In the **Elan_Rev B AM386SC300**, the following pins have had their Suspend Modes states changed:

Table 7. Suspend Mode Output Pin States

Pin No.	Signal Name	Suspend Mode State	Comments
45	SYSCLK	0	This output used to go high in Suspend Mode in the Elan Rev A.
200	X1OUT/[BAUDOUT]	0	This output will go low in Suspend Mode when configured as the 14MHz clock output (X1OUT).
200	X1OUT/[BAUDOUT]	last state	When configured as the Baudrate clock output, the state of this pin will not change in Suspend Mode.
200	X1OUT/[BAUDOUT]	tri-state	When this pin is not enabled, it will remain tri-stated in Suspend Mode.

Micro Power OFF Mode

The following paragraphs describe the Elan Rev B in Micro Power OFF Mode.

Micro Power R.T.C. And Dram Interface Usage

The following are distinctive characteristics:

- Minimum power mode of Élan (target is 15µA typical, AVCC and Core Vcc combined).
- Allows the system designer to utilize the internal Élan RTC and RTC RAM to maintain time, date, and system configuration data while other system peripherals are powered off.
- Provides the system designer with the option of keeping the system DRAM powered and refreshed while other system peripherals are powered off. Self refresh and CAS# before RAS# refresh DRAMs are supported.
- Minimal external logic required to properly control power supplies and/or power switching.
- No external buffering required to properly power down system hardware.

- One pin added to Élan (IORESET#).
- Minimal backward compatibility issue with Rev A~~x~~ Élan.

The Élan Rev B contains modifications such that a system designer can easily maintain the internal RTC and RTC ram and optionally, the DRAM interface to maintain DRAM refresh, while the rest of the system peripherals attached directly to Élan are powered off. All Élan power pins associated with the I/O pins of external powered off peripherals must be powered down also. This in addition to some internal Élan termination, provides the required isolation to allow the external peripherals to be powered off.

A single pin was added to Élan Rev B, IORESET# (Input Output Reset). In addition, auto-matically controlled internal I/O termination was also added to terminate the device's internal nodes properly when required. The new pin IORESET# is pin # 140 in the Élan Rev B device.

The DRAM CAS# before RAS#, or self refresh can be maintained by Élan in this Micro Power state, if configured to do so, utilizing the 32kHz clock used by the RTC and a portion of the Élan core logic. The VMEM power plane of Élan (DRAM / SRAM section power) must remain powered on if the CAS# before RAS# refresh option is selected while in the Micro Power state. The VMEM power plane of Élan must also remain powered on if the self refresh option is selected and the specific DRAM device requires any of its control pins (ie WE#) to remain inactive in the self refresh mode.

A portion of a typical system using a secondary power supply to maintain the RTC and RTC RAM (and optionally system DRAM) is shown in Figure 2. This secondary power supply could be as simple as a small lithium coin cell battery as indicated in the diagram, but is certainly not limited to this. Lithium coin cell useage will be dependent on the Élan Rev B low voltage characterization. The AVCC and VCC(CORE) minimum target is 2.4 volts. Note that when all primary power supply outputs are turned off, all of the system's peripherals are powered off (DRAM optional), all of Élan's power planes are powered off except AVCC (analog) and Vcc (core), and the secondary power supply is "switched in" to maintain Élan's core and analog power source.

The RESIN# pin acts as the Élan master reset. When active, all of the Élan internal components are reset including the RTC and the RTC ram invalid bit will be set. Therefore, the RESIN# pin should only be asserted (pulsed) low when a power source is initially applied to Élan's core and analog sections. The IORESET# signal is intended to be the normal "POWER GOOD" status from the primary power supply in this example design. The IORESET# input to Élan does not reset the RTC and will not set the RTC ram invalid bit. IORESET# (when the inactive state is detected) will cause Élan to go through its power up sequence including phase lock loop start up for clock generation and an internal CPU reset. See Figure 3 for the reset and power timing requirements on the initial Élan power up, and on Micro Power mode exit.

When the primary power supply outputs are turned off, all of Élan's powered down I/O pins, are essentially tri-stated and the internal pullups are removed because the output driver's VCC I/O and VCC CLAMP have been removed (See Figure 4). This provides the ability to power off external peripherals that are attached directly to Élan without concern of Élan driving current into the pins of the external powered down device. In order to assure that Élan does not draw excessive power while in this state, internal pull-down resistors will be enabled so as not to cause the input buffers to float. See the FORCE TERM signal in Figure 4.

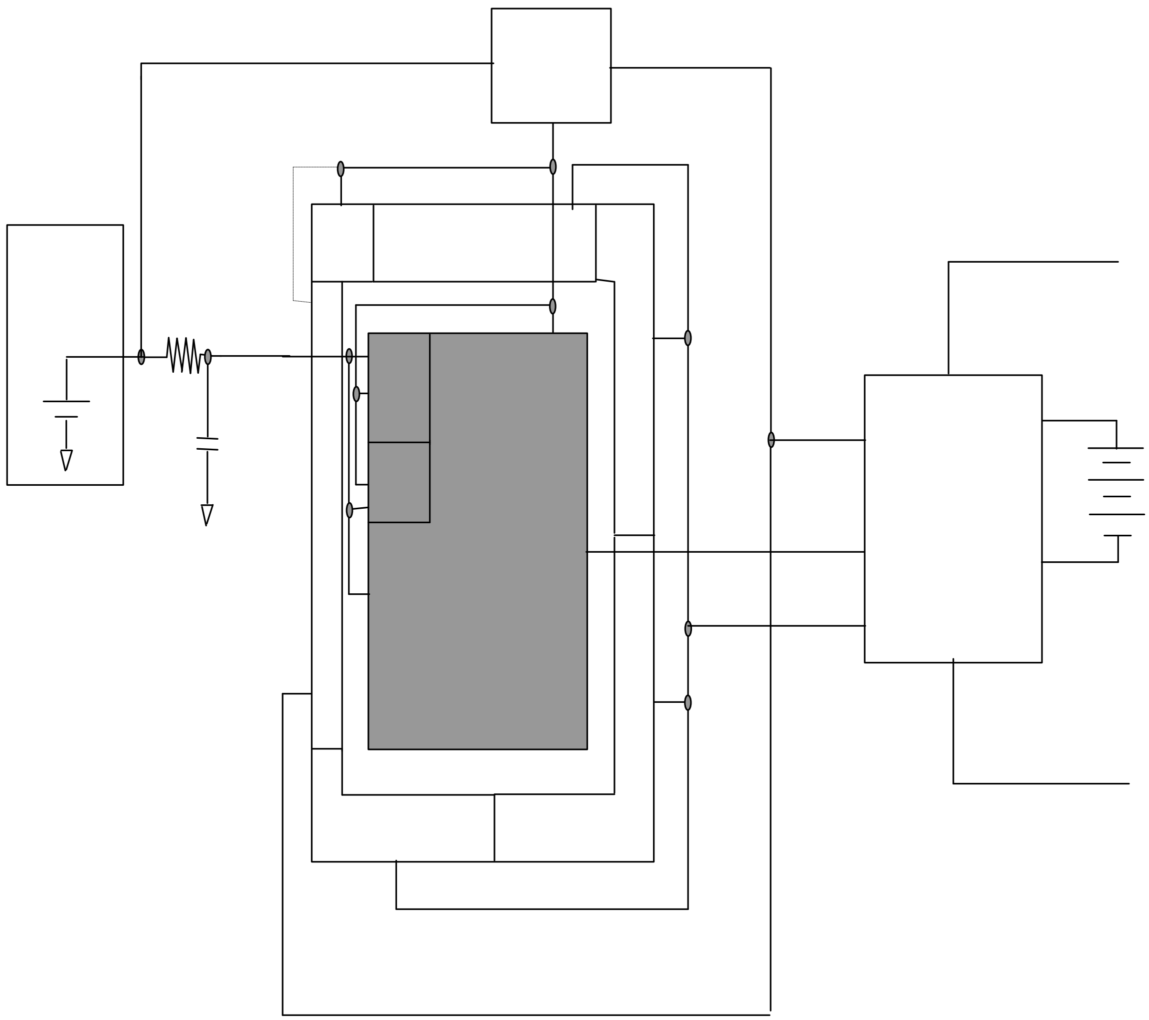


Figure 2. Typical System Design With Secondary Power Supply To Maintain RTC When Primary Power Supply Is Off DRAM Refresh Is Optional

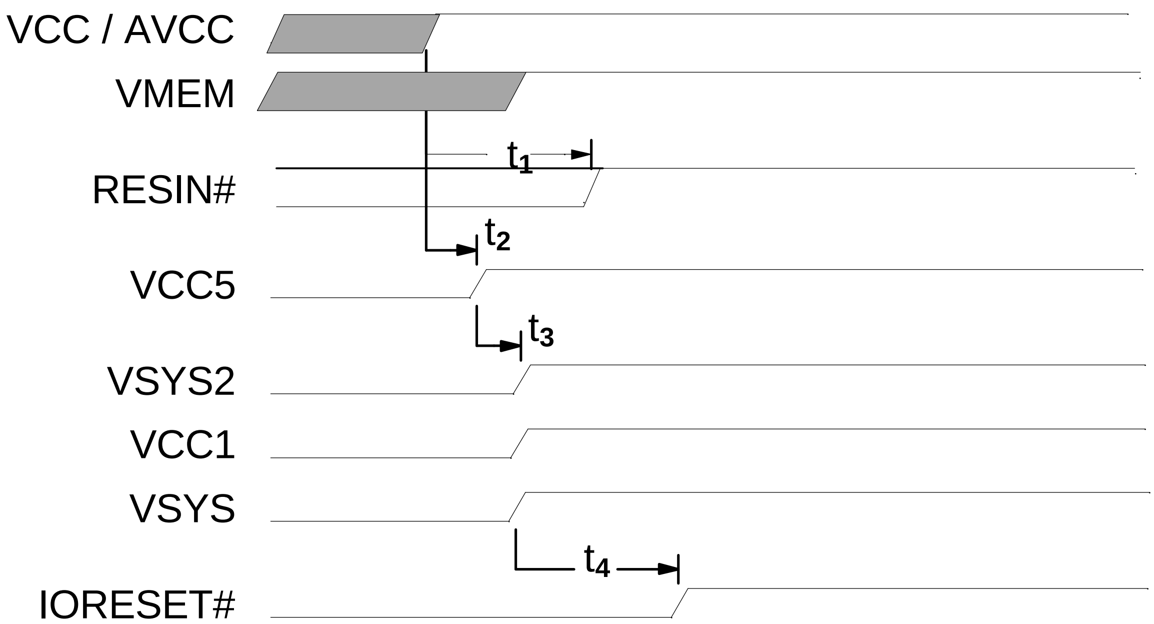


Figure 3. RESIN# and IORESET# Timing On Initial Power Up and on Micro Power Mode Exit

Name	Description	Min	Max
t_1	Core and analog Vcc, and optionally VMEM, valid to RESIN# inactive	TBD	-
t_2	Core and analog Vcc valid to VCC5 valid delay	TBD	-
t_3	VCC5 to VSYS2,VCC1,VSYS, and optionally VMEM delay	TBD	-
t_4	VSYS2,VCC1,VSYS, and optionally VMEM valid to IORESET# inactive	TBD	-

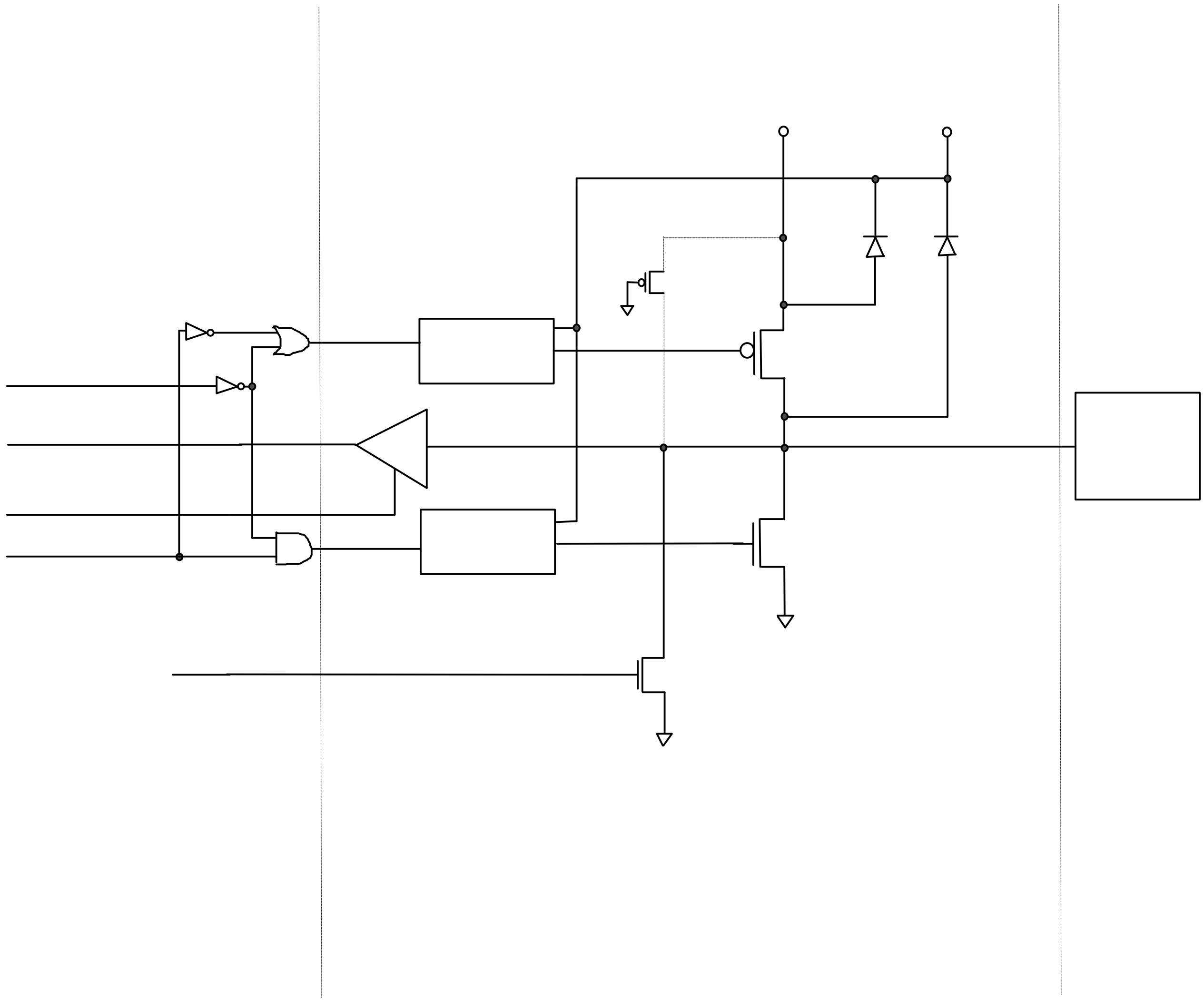


Figure 4. Élan Rev B I/O structure

WHERE: VCC I/O = VCC5 or VMEM or VSYS or VSYS2 or AVCC or VCC1
VCC CLAMP = VCC5 or VMEM or AVCC

The Élan Rev B samples the two reset inputs to logically determine what state the Élan power pins are in and in turn control the internal pull-down resistors. Table 8 outlines this functionality.

Table 8. Internal I/O Pull-Down States

IORESET#	RESIN#	FORCE TERM	COMMENTS
0	0	ACTIVE	This condition occurs when secondary power supply is initially turned on and all other power sources are off. Élan's core and analog Vcc is transitioning to on and RESIN# is active
0	1	ACTIVE	This condition occurs when the core and analog Vcc is stable, the RESIN# pin has been inactive and the primary power supply outputs are off
1	0	ACTIVE	This condition should be treated as condition 0,0 above
1	1	INACTIVE	This occurs when the secondary power supply is on, the RESIN# input is inactive and the primary power supply is on and has deasserted IORESET#

Micro Power DRAM Refresh

The system designer has the option to keep the system DRAM powered up and refreshed while Élan is in this "micro power state". A configuration bit was added to the Élan PMU section of the core logic to realize this feature, called the Micro Power Refresh Enabled bit. This bit is bit 2 of the Configuration Register at Index BAH. If this bit is cleared (default), the core logic associated with the DRAM refresh will be disabled when Élan is in the micro power state. If the bit is set, the core logic associated with the dram refresh will be enabled and functional while Élan is in its micro power state.

The type of DRAM refresh (CAS# before RAS# or self refresh) that will be performed during Micro Power mode will be the same as that which Élan was configured for in Suspend Mode prior to the IORESET# pin being sampled low. If the micro power refresh feature is enabled for CAS# before RAS# refresh, the system designer should maintain power on the VMEM power pin of Élan and not remove power from the DRAM devices. If the micro power refresh feature is enabled for self refresh, the system designer may or may not be required to maintain power on the VMEM power pin of Élan depending on the specific requirement of the DRAM device in self refresh mode. Power should not be removed from the DRAM device itself in either case.

The Micro Power Refresh bit will always be cleared whenever the RESIN# input is sampled low. Therefore, when the core is initially powered up, the Micro Power DRAM refresh feature will be disabled. This bit is not affected by the IORESET# input. This bit will provide the system BIOS with a mechanism to determine whether or not the system DRAM data has been retained after a reset (IORESET#) has occurred.

If self refresh mode is selected and is enabled for Micro Power mode, then when Micro Power mode is exited Élan will properly force a CAS# before RAS# refresh cycle to cause the DRAMs to exit the self refresh mode and then transition to the normal CAS# before RAS# refresh mode. This functionality is exactly the same as the self refresh mode exit when the CPU ~~c~~Clock ~~s~~Stopped mode is exited. Élan is currently designed to only generate one CAS# before RAS# refresh cycle to force the DRAM to exit the self refresh mode. This also true for the Micro Power DRAM refresh feature.

The timing diagrams in Figures 5 and 6 show the required sequence of events that is required in order to guarantee a proper transition into the Micro Power state. This is especially critical when the DRAM refresh option is selected in order not to destroy any data. Note that it is required to keep the power pins of Élan stable for some time after the IORESET# input has gone active. Stable implies that these power pins should remain at least at there VCC (min) value for the specified time indicated below.

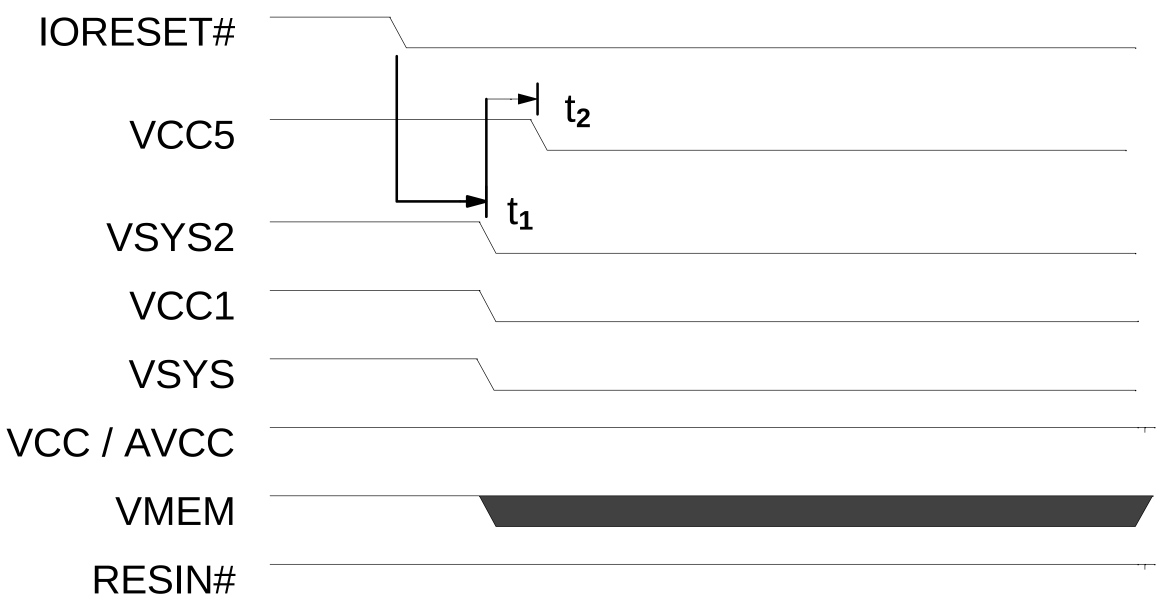


Figure 5. Entering Micro Power, DRAM Refresh Disabled

Name	Description	Min	Max
t_1	VCC5, VSYS2, VCC1, VSYS hold time from IORESET# inactive	5 µs	-
t_2	VCC5 hold time from VSYS2, VCC1, VSYS inactive	0 ns	-

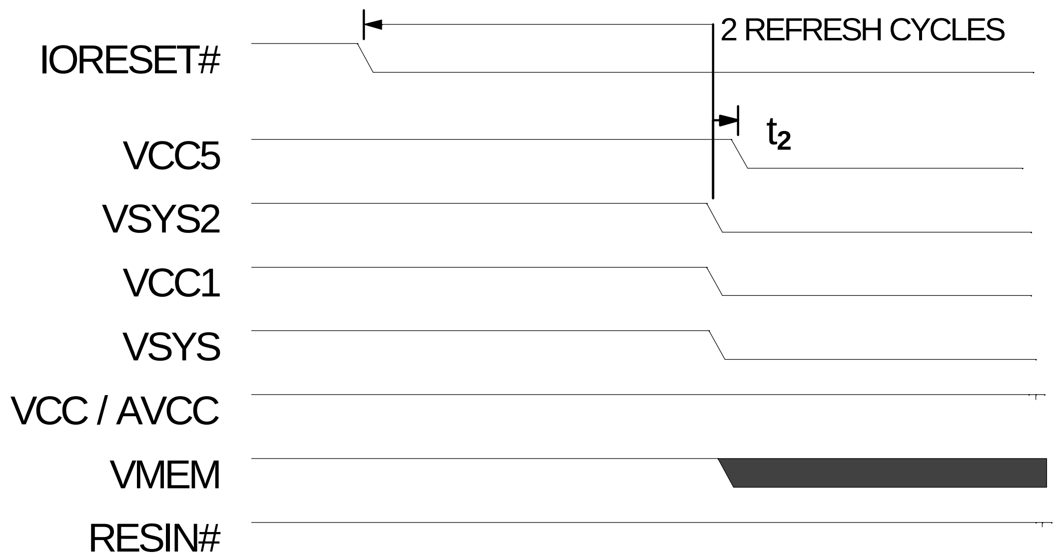


Figure 6 - Entering Micro Power, Dram Refresh Enabled CAS# Before RAS# Or Self Refresh

Name	Description	Min	Max
2 REFRESH CYCLES	VCC5, VSYS2, VCC1, VSYS hold time from IORESET# inactive	-	-
t_2	VCC5 hold time from VSYS2, VCC1, VSYS inactive	0 ns	-

Note: 2 Refresh Cycles implies that the Vcc rails of Élan must remain stable after the IORESET# input is driven active for a minimum time that is equal to the Élan internal refresh period. As an example, if the internal refresh timer source was programmed for a 125µs period, then the Élan Vcc sources described above would be required not to drop below the specified Vcc (min) for a minimum of 250µs after the IORESET# input goes active.

Élan Power Pins

The Élan Rev B power pins have been reconfigured and now have the functionality shown:

VCC	(Core Logic Vcc) (VCC IO for pin 141 RESIN#) (VCC CLAMP for pin 141 RESIN#)
VCC5	(VCC IO for I/O pins 80 - 140) (VCC CLAMP for I/O pins 43 - 140 and 143 - 200)
VSYS2	(VCC IO for I/O pins 143 - 161)
VCC1	(VCC IO for I/O pins 162 - 200).
VMEM	(VCC IO for I/O pins 2 - 42) (VCC CLAMP for I/O pins 2 - 42)
VSYS	(VCC IO for I/O pins 43 - 79)
AVCC	(VCC IO for I/O pins 201 - 207) (VCC CLAMP for I/O pins 201 - 207)

Internal Pull-Down Resistors

None of the pins associated with the analog section of Élan (AVCC), IORESET#, or the RESIN# input pin has an internal pull-down resistor. The pins associated with the Élan memory interface (VMEM) have internal pull-downs. These memory interface pins are pulled down if the micro power DRAM refresh is disabled,and Élan is in the micro power state. If Micro Power DRAM refresh is enabled, only the MA10-MA0 and D15-D0 are pulled down, with the remaining DRAM interface pins either active or driven out to maintain the DRAM refresh.

All remaining Élan I/O pins not associated with the analog or memory interface have the internal pull-down resistor attached to the pad when Micro Power mode is entered.

Core and Analog Micro Power D.C. Characteristics

The target for the Élan Rev B Micro Power mode design is:

VCC (min.) = 2.4 V~~v~~
AVCC(min) = 2.4 V~~v~~

These values are currently under investigation.

Bus Option Select Pins

The serial port interface pins, DTR#, RTS# and SOUT are sampled by Élan at power up to determine the Élan bus option : Internal LCD controller, Local Bus, or Maximum ISA. These pins are required to be terminated externally with pull-up or pull-down resistors corresponding to the bus option that is desired. In the Élan Rev B design, any pull-up resistor used to terminate these pins should have a value of 10K ohms (maximum). Any pull-down resistor used to terminate these pins should have a value of 100k ohms minimum.

ISA Bus Controller

This section documents the changes that have been made in the Élan Am386SC300 **Rev B** ISA Bus Controller.

MCS16# Timing

In the Élan Rev A, MCS16# is latched at the end of the first T2 cycle or the end of T1P. The clock switching logic does not guarantee that the CPUCLK will switch to low speed during that time. If the Élan Rev A is in Internal LCD controller or Local Bus mode, there are LA23-LA17 address lines external to the Élan. In these cases, an external device would have less than 10ns to return MEMCS16. For the Élan Rev B, MEMCS16 is not latched and the CPUCLK will always switch to low speed properly.

If the Élan Rev A is in FULLISA mode, an external device has less than 20ns to return MCS16#. In the Élan Rev B Am386SC300 design, the CPUCLK will switch to low speed before latching MCS16#. This will allow the Élan Rev B to have ISA compatible timing.

Bits 2 and 3 of the ROM Configuration Register 2, Index 51H, are “reserved: (must be one) in the Élan Rev A. In the Rev B, these bits are tied off. Setting or clearing these bits in Élan Rev B has no effect.

Port 80H I/O Cycles

In the Élan Rev A, I/O writes to Port 80H do not cause the data to be propagated to the SD bus because the DBUFOE# signal is not generated on this cycle. For the Élan Rev B, the write data will be associated with DBUFOE# going active, allowing data to go out to the SD bus. Reads from I/O Port 80H still source data from an internal register.

Phase Locked Loops

The video PLL output frequency in the Élan Am386SC300 RevB changed from 14.746MHz to 14.336MHz. This frequency is used by the internal CGA Controller and may also be used by external devices by programming the X1OUT/[BAUDOUT] pin to provide X1OUT.

Elan XT Keyboard

The XT keyboard interface in Elan (Rev B) is compatible with the IBM(R) PC-XT(R) keyboard, consisting of clock and data inputs to Elan. One of the other output pins, such as a PGP pin may be used as the reset output, if it is desired to drive an actual XT keyboard reset input. Refer to sections 2.6.1 and 2.6.5 for an explaination of pin option tradeoffs.

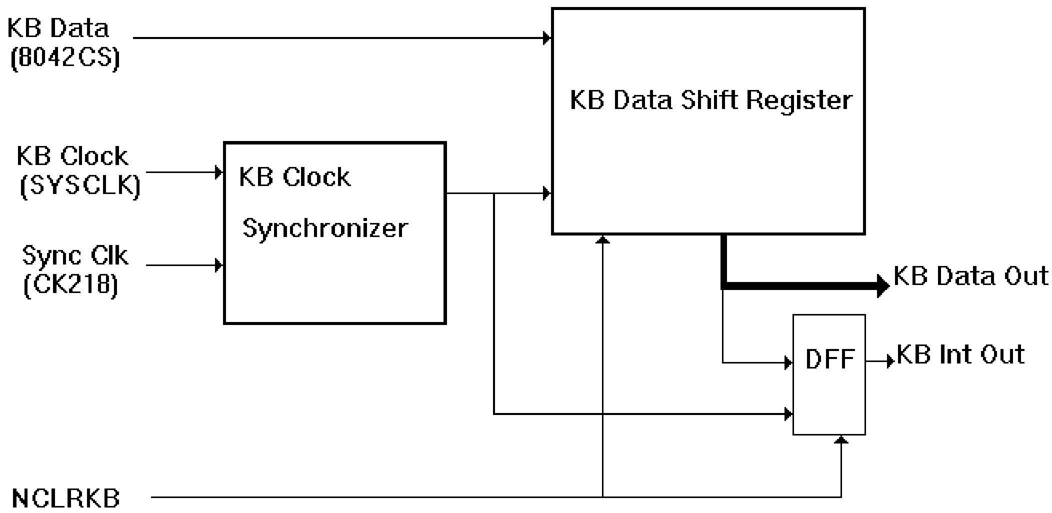


Figure 7. XT Keyboard Block Diagram

The clock input becomes synchronized by two serial flip-flops which are clocked by a signal called CK218. This signal is actually the CPU clock signal divided by 6. The (thus delayed) KB clock signal is then used to clock the data into the KB Data Shift Register. The first bit to be clocked in will be considered the start bit, and must be a logic '1' (high). Eight more bits are then shifted in, beginning with the lsb. On the ninth clock, the start bit is shifted into the DFF which drives the KB interrupt output, which connects to IRQ1. At this same time, the KB Data In pad changes directions to become an output, and is driven low, as a "busy" indication to the keyboard or other driving device. At this time, the host should respond to the interrupt, and should read the byte assembled in the KB Data Shift Register at port 060H. The host also has the option of driving the clock pin low as an additional handshake indication. After the host has read the byte from port 060H, the host clears the KB Data Shift Register and the Interrupt Flip Flop by writing port 061H bit 7 high, then low again. This action not only clears the shift register and interrupt, but also releases the Data Line to be an input again.

XT Keyboard Enable

The enable bit for the XT keyboard circuitry in the Elan Rev B is at Index 0ADH, bit 3. When this bit is set, it does several things:

1. Allows the pins (8042CS# and SYSCLK) to become tristated, so that they may be used as inputs (all other requirements being met).
2. Qualifies an internal decode so that port 60 will be read as an internal port.
3. Switches a multiplexor to vector IRQ1 from the external pin to the output of this circuitry.

Keyboard Interface Control

Two control bits are provided for control of the XT keyboard interface. These are located at Port 61, and are the two most significant bits. Bit 7 is used to clear the keyboard interrupt and shift

register, and also a flip-flop that enables the data line as an output, which will be low), to be used as a “busy” signal to the keyboard. Two writes are required for the proper operation of this bit: the first to set it, and the second to clear it. (If it is not cleared, then the shift register will be held in a “clear” configuration). Bit 6, when high, will make the KBCLK line an output (driving it low), which can also be used as a “busy” signal to the keyboard.

Keyboard Data Port

Once a serial keyboard byte has been assembled, it can be read at Port 60.

I/O Map Summary

Index ADH, bit 3 set	-	Enable XT keyboard
Port 60	-	Keyboard Data
Port 61, bit 7	-	Clear KB shift register & interrupt
Port 61, bit 6	-	Force KB clock low

Pins Used

The XT Keyboard option uses the following pins:

SYSCLK - becomes KB clock (input)
CS8042# - becomes KB data (input)

Since both of these pins can also drive as outputs, and the data line will be driven as an output at the end of each byte transferred, they must be driven by open drain or open collector drivers with external pullups.

Timing (General)

The XT keyboard clock runs at roughly 100 kHz, or 10 µSec per bit. The falling edge of the XTCLKinput (after being delayed by two cpuclks/6) is what clocks the shift register. Therefore, XTDAT should be changed on the rising edge of the XTCLK signal. Elan Rev B XT keyboard interface will run at speeds up to 250 kHz.

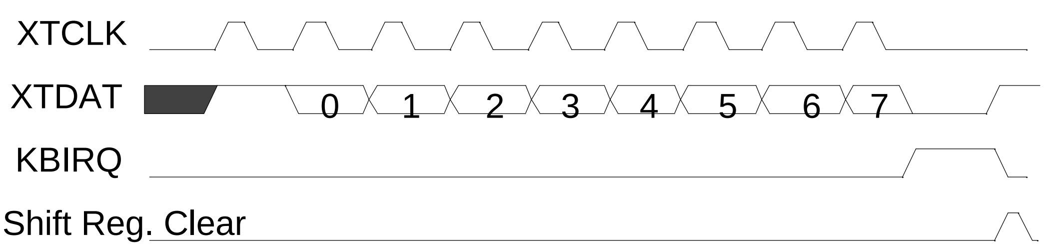


Figure 8. XT Keyboard Timing Diagram

Configuration (Index) Registers

This section documents the changes that have been made in the Élan Am386SC300 Rev B Configuration Registers. Programmable control, or Configuration Registers at Index B1H, B3H, and B4H were modified. Registers at Index B5H, B6H, B7H, B8H, B9H, and BAH were added.

Miscellaneous Control Register 3, Index ADH

In the Élan Rev B, a new value has been added for bit 3 (XTKBEN) of this register, as shown in the following table.

Table 9. Index ADH Bit Values

Bit No.	Bit Name	Read/Write	Function
7-4		R/W	Same as for Élan Rev
3	EB_RMMD1	R/W	Enables XT Keyboard Interface when set
2-0		R/W	Same as for Élan Rev A

Function Enable Register 2, Index B1H

Values for bits 7-6 of the Function Enable Register 2, Index B1H have been added in Rev B. When bit 7 of the Configuration Register at Index B4H is set, the values of bits 6 and 7 of Index B1H determine the Élan Am386SC300 RAM mode as shown in the following tables.

Table 10. Index B1H Bit Values

Bit No.	Bit Name	Read/Write	Function
7	EB_RMMD0	R/W	Élan Rev B RAM mode select bit 0
6	EB_RMMD1	R/W	Élan Rev B RAM mode select bit 1
5-0		R/W	same as Élan Rev A

Table 11. RAM Mode Decode Logic

RAM Mode	Index B4H bit 7	Index B1H [7:6]	Total Memory	Bank0	Bank1
	0	X X	Determined by Index 66H,[4:2]		
256K Type Bank Mode	1	0 0	512K	512K	-
256K Type Bank Mode	1	0 1	1M	512K	512K
Asymmetric type 1Mx16 bit DRAM Mode	1	1 0	2M	2M	
Asymmetric type 1Mx16 bit DRAM Mode	1	1 1	4M	2M	2M

Notes: 1. If bit 7 of Index B4H is set, bits 4:2 of Memory Configuration Register, Index 66H are disabled. Bits 0-1 of Index 66H determine page mode or enhanced page mode.

2. If the 4M memory configuration is selected, the enhanced page mode MUST be selected via bits 0-1 of Index 66H

Status Readback Register, Index B3H

The functionality of bit 0 of the Status Readback Register, Index B3H, changed and values for bits 2 -6 were added.

Table 12. Index B3H Bit Values

Bit	Name	R/W	Function

7		R	Same as Élan Rev A
6	ENFROMCS	R/W	Enable ROMCS accesses to run at the high speed CPU clock rate.
5	FBROMWS1	R/W	Fast ROMCS wait-state select 1
4	FBROMWS0	R/W	Fast ROMCS wait-state select 0
3	ENSELFRF	R/W	Enable self-refresh DRAM mode when CPUCLK is stopped
2	ENBROMCS	R/W	ROMCS# output is an address decode, not qualified with MEMR# or MEMW#.
1	EXTSMISTE	R	Same as Élan Rev A
0	EXTSMISTA	R/W	External SMI status 1 = External SMI occured. Cleared by Reset or a write of 0 to this bit

PCMCIA Setup Register, Index B4H

Values for bits 6 and 7 of the PCMCIA Setup Register, Index B4H, were added.

Table 13. Index B4H Bit Values

Bit	Name	R/W	Function
7	ENRAME2	R/W	Enable Élan Rev B RAM modes. See Index B1[7:6].
6	ENEMSCA	R/W	Enable the ability to control PCMCIA address bits 24 &25 for every possible PCMCIA MMS window. (see Registers at Index B5H, B6H, and B7H).
5-0		R/W	Same as Élan Rev A

Configuration Register, Index B5H

In the Élan Am386SC300 RevB, Index B5H is a new register.

Table 14. Index B5H Bit Values

Bit	Name	R/W	Function
7	MMSAP325	R/W	MMSA page 3 CA25
6	MMSAP324	R/W	MMSA page 3 CA24
5	MMSAP225	R/W	MMSA page 2 CA25
4	MMSAP224	R/W	MMSA page 2 CA24
3	MMSAP125	R/W	MMSA page 1 CA25
2	MMSAP124	R/W	MMSA page 1 CA24
1	MMSAP025	R/W	MMSA page 0 CA25
0	MMSAP024	R/W	MMSA page 0 CA24

Configuration Register, Index B6H

In the Élan Am386SC300 RevB, Index B6H is a new register.

Table 15. Index B6H Bit Values

Bit	Name	R/W	Function
7	MMSAP725	R/W	MMSA page 7 CA25
6	MMSAP724	R/W	MMSA page 7 CA24

5	MMSAP625	R/W	MMSA page 6 CA25
4	MMSAP624	R/W	MMSA page 6 CA24
3	MMSAP525	R/W	MMSA page 5 CA25
2	MMSAP524	R/W	MMSA page 5 CA24
1	MMSAP425	R/W	MMSA page 4 CA25
0	MMSAP424	R/W	MMSA page 4 CA24

Configuration Register, Index B7H

In the Élan Am386SC300 RevB, Index B7H is a new register.

Table 16. Index B7H Bit Values

Bit	Name	R/W	Function
7	MMSBP325	R/W	MMSB page 3 CA25
6	MMSBP324	R/W	MMSB page 3 CA24
5	MMSBP225	R/W	MMSB page 2 CA25
4	MMSBP224	R/W	MMSB page 2 CA24
3	MMSBP125	R/W	MMSB page 1 CA25
2	MMSBP124	R/W	MMSB page 1 CA24
1	MMSBP025	R/W	MMSB page 0 CA25
0	MMSBP024	R/W	MMSB page 0 CA24

Configuration Register, Index B8H

In the Élan Am386SC300 RevB, Index B8H is a new register.

Table 17. Index B8H Bit Values

Bit	Name	R/W	Function
7	ENFSTRDOS	R/W	Enable ROMDOS accesses to run at the high speed CPU clock rate.
6	FRDOSWS1	R/W	ROMDOS wait state select 1
5	FRDOSWS0	R/W	ROMDOS wait state select 0
4	ENRDOSCS	R/W	DOSCS is an address decode. It is not qualified withMEMR# or MEMW#.
3	RDOSSIZ3	R/W	ROMDOS size select 3
2	RDOSSIZ2	R/W	ROMDOS size select 2
1	RDOSSIZ1	R/W	ROMDOS size select 1
0	RDOSSIZ0	R/W	ROMDOS size select 0

Table 18. ROMDOS Size Select Logic

RDOSSIZ[3:0]	DOSCS# Address Decode	DOS ROM Size
0 0 0 0	DOSCS# uses MMS mapping	n/a
0 0 0 1	F00000H - FEFFFFH	~1MB
0 0 1 0	E00000H - FEFFFFH	~2MB
0 0 1 1	D00000H - FEFFFFH	~3MB
0 1 0 0	C00000H - FEFFFFH	~4MB
0 1 0 1	B00000H - FEFFFFH	~5MB
0 1 1 0	A00000H - FEFFFFH	~6MB
0 1 1 1	900000H - FEFFFFH	~7MB
1 0 0 0	800000H - FEFFFFH	~8MB
1 0 0 1	700000H - FEFFFFH	~9MB
1 0 1 0	600000H - FEFFFFH	~10MB
1 0 1 1	500000H - FEFFFFH	~11MB
1 1 0 0	400000H - FEFFFFH	~12MB
1 1 0 1	300000H - FEFFFFH	~13MB
1 1 1 0	200000H - FEFFFFH	~14MB
1 1 1 1	100000H - FEFFFFH	~15MB

Table 19. ROMDOS Enable and Wait-State Select Logic

ENFSTRDOS	FRDOSWS[1:0]	# of Wait-States for DOSCS# cycle
0	X X	Same as Élan Rev A
1	0 0	4
1	0 1	3
1	0 0	2
1	1 1	1

Configuration Register, Index B9H:

In the Élan Am386SC300 RevB, Index B9H is a new register.

Table 20. Index B9H Bit Values

Bit	Name	R/W	Function
7	DISREFOFF	R/W	Disable Refresh in the PMU Off Mode
6	**Reserved**		Reserved
5	MEMDATS1	R/W	D(15:0) drive strength select 1
4	MEMDATS0	R/W	D(15:0) drive strength select 0
3	MEMADRS1	R/W	MA(10:0)/SA(13:23), MWE#, drive strength select bit 1
2	MEMADRS0	R/W	MA(10:0)/SA(13:23), MWE#, drive strength select bit 0
1	MEMCTLS1	R/W	RAS0#, RAS1# drive strength select 1
0	MEMCTLS0	R/W	RAS0#, RAS1# drive strength select 0

Table 21. Output Drive Strength Select Logic

The values of output drive strength types are shown in Table 1.

Drive Strength Select Bit Value Select 1	 Select 0	Output Drive Strength
0	0	E
0	1	C
1	0	D
1	1	tri-state output

Configuration Register, Index BAH:

In the Élan Am386SC300 RevB, Index BAH is a new register.

Table 22. Index BAH Bit Values

Bit	Name	R/W	Function
7-5	Reserved		Reserved
4	EN_MCE_PP	R/W	Enable PCMCIA MEM commands on Parallel Port Pins
3	EN_14M_PP	R/W	Enable 14M Clock output on AFDT#, pin 80
2	EN_mPOM	R/W	Enable micro power refresh mode
1:0	Reserved		Reserved

Version Register, Index 64H

The Élan Version Register, read of Index 64H, has been changed from a value of 1 to a value of 2 (decimal).

IOCHCHK polarity at Port B

Bit 5 of the Port B register, IOCHCHK status bit, indicates error status when the Élan Rev A is configured in Local Bus and Internal CGA modes. This bit will read as a 0 for Local Bus and Internal CGA modes for the Élan Am386SC300 Rev B.

Note: This is not backward compatible with the Élan Rev A.

CA24 and CA25 Control Registers

To provide more flexibility with the PCMCIA mapping scheme, the capability to set the state of CA24 and CA25 for each MMS page (or Window) has been added. In the previous version of the Élan, CA24 and CA25 were set on a socket basis. All accesses to one of the PCMCIA sockets would have CA24 and CA25 in the same state, accessing the same 16M block, regardless of which MMS Window or Page was used in the access.

In the Élan Am386SC300 Rev B, it is possible to map accesses to different pages to access anywhere in the PCMCIA 64M memory map. The power-up state is 100% compatible with the Élan Rev A. Bit 6 of the Configuration Register, Index B4H, is the enable bit for this functionality. If this bit is cleared (default state), CA24 and CA25 are controlled by the logic that exists in the Élan Rev A design. If this bit is set, registers at Index B5H, B6H, and B7H control the two output pins as follows:

Table 22. Index B5H, B6H and B7H Bit Values

Bit No.	INDEX B5H		INDEX B6H		INDEX B7H	
0	MMSA page 0	CA24	MMSA page 4	CA24	MMSB page 0	CA24
1	MMSA page 0	CA25	MMSA page 4	CA25	MMSB page 0	CA25
2	MMSA page 1	CA24	MMSA page 5	CA24	MMSB page 1	CA24
3	MMSA page 1	CA25	MMSA page 5	CA25	MMSB page 1	CA25
4	MMSA page 2	CA24	MMSA page 6	CA24	MMSB page 2	CA24
5	MMSA page 2	CA25	MMSA page 6	CA25	MMSB page 2	CA25
6	MMSA page 3	CA24	MMSA page 7	CA24	MMSB page 3	CA24
7	MMSA page 3	CA25	MMSA page 7	CA25	MMSB page 3	CA25

Port 92H

The Élan Rev B Am386SC300 has an added Port 92 implementation.

Bit No.	Bit Name	R/W	Function	Default
7-2	Reserved		Reserved (Read 0s)	0
1	GATEA20	R/W	When this bit is 0 and all other gatea20 sources are de-asserted, system address bit 20 (SA20) is forced low	0
1	HOTRST	R/W	A low to high transition in this bit will automatically reset the CPU. The reset will last for 16 CPU clock cycles	0

Note: In earlier Élan design, writing to Port 92 writes the DMA Channel 3 page register. For the current Élan Rev B design, only I/O accesses in the range 0080H - 008FH access the DMA page registers.

JTAG Software

The original Élan design used a noncombined Bidirectional cell. The effects are that during a sample/preload test for every bidirectional pad cell an additional shift must be performed to load data in all the boundary cells. The total number of shifts required for Élan Rev A is 219, and for Élan Rev B it is 173. Two pins were changed from outputs to bidirectional in the Élan Rev B, the 8042CS# and SYSCLK pin. Table 25 shows the JTAG cells.

Table 25. Boundary Scan (JTAG) Cells. Order and Type.

Pin No.	Name	Cell Type	Notes
77	pmc(2)	output	
78	xrc	input	
79	a20gate	input	
80	xafd	output	
82	pe	input	
83	xstrb	output	
84	xslctin	output	
85	busy	input	
86	xerror	input	
87	slct	input	
88	xack	input	
89	xinit	output	
90	xppdwe	bidir	
91	xppoen	bidir	
92	xdtr	bidir	
93	xrts	bidir	
94	sout	bidir	
96	xcts	input	
97	xdsr	input	
98	xdcd	input	
99	sin	input	
100	xrin	input	
101	acin	input	
102	extsmi	input	
103	resume	input	
*	*	control	Control cell for pins 106 to 155
106	xbl1	input	
107	xbl2	input	
108	xbl3	input	
109	xbl4	input	
110	xcda	input	
111	xrdya	input	
112	wpa	input	
113	bvd2a	input	
114	bvd1a	input	
115	xwaitab	input	
116	xcdb	input	
117	xrdyb	input	
118	wpb	input	
119	bvd2b	input	
120	bvd1b	input	
122	icdir	output	
123	xmcelb	output	
124	xmcehb	output	
125	vppb	output	
126	xregb	output	
127	rstb	output	
129	xmcela	output	
130	xmceha	output	
131	vppa	output	

132	xrega	output	
133	rsta	output	
134	ca24	output	
136	ca25	output	
137	pmc(0)	output	
138	pmc(1)	output	
139	spkr	output	
140	mainclock	input	
141	xresin	input	
143	sbhe	output	
144	di_r	output	
145	lvdd	output	
146	xdsce	output	
147	xdsoe	output	
148	dsmd(0)	bidir	
149	dsma(14)	output	
150	dsma(13)	output	
151	dsma(12)	output	
152	dsma(11)	output	
153	dsma(10)	output	
154	dsma(9)	output	
155	dsma(8)	output	
*	*	control	Control cell for pins 158 to 200
158	dsma(7)	output	
159	dsma(6)	output	
160	dsma(5)	output	
161	dsma(4)	output	
162	dsma(3)	output	
163	dsma(2)	output	
164	dsma(1)	bidir	
165	dsma(0)	output	
166	dsmd(1)	bidir	
167	dsmd(2)	bidir	
168	dsmd(3)	bidir	
169	dsmd(4)	bidir	
170	dsmd(5)	bidir	
171	dsmd(6)	bidir	
172	dsmd(7)	bidir	
173	m	bidir	
174	d0_i	bidir	
175	d2_g	bidir	
177	d3_b	bidir	
178	cp1_hdrv	bidir	
179	cp2_vdo	bidir	
181	frm_vdrv	bidir	
182	lvee	bidir	
183	xdswe	bidir	
184	pmc(4)	output	
185	pmc(3)	output	
186	pgp(3)	bidir	
187	pgp(2)	bidir	
188	pgp(1)	bidir	
189	pgp(0)	bidir	

190	xlph	output	
191	iochrdy	input	
193	pirq(1)	input	
194	pirq(0)	input	
195	irq1	input	
196	xiocs16	bidir	
197	xmcs16	bidir	
198	irq14	bidir	
200	clk14_o	output	
*	*	control	Control cell for pins 2 to 51
2	xras0	output	
3	xras1	output	
4	xcas1l	output	
5	xcas1h	output	
6	xcas0l	output	
7	xcas0h	output	
8	xmwe	output	
10	ma(10)	output	
11	ma(9)	output	
13	ma(8)	output	
14	ma(7)	output	
15	ma(6)	output	
16	ma(5)	output	
17	ma(4)	output	
18	ma(3)	output	
19	ma(2)	output	
21	ma(1)	output	
24	ma(0)	output	
25	d(15)	bidir	
26	d(14)	bidir	
27	d(13)	bidir	
28	d(12)	bidir	
29	d(11)	bidir	
30	d(10)	bidir	
31	d(9)	bidir	
32	d(8)	bidir	
34	d(7)	bidir	
36	d(6)	bidir	
37	d(5)	bidir	
38	d(4)	bidir	
39	d(3)	bidir	
40	d(2)	bidir	
41	d(1)	bidir	
42	d(0)	bidir	
43	xrdoscs	output	
44	xromcs	output	
45	sysclk	bidir	
46	xdack2	*	This pin becomes TCK when JTAGEN is high.
47	aen	*	This pin becomes TDI when JTAGEN is high.
49	tc	*	This pin becomes TMS when JTAGEN is high.
50	endirl	output	

51	endirh	output	
*	*	control	Control cell for pins 54 to 103
54	xior	output	
55	xiow	output	
56	xmemr	output	
57	xmemw	output	
58	rstdrv	output	
59	xdbufoe	output	
60	sa(12)	output	
61	sa(11)	output	
62	sa(10)	output	
63	sa(9)	output	
64	sa(8)	output	
66	sa(7)	output	
67	sa(6)	output	
69	sa(5)	output	
70	sa(4)	output	
71	sa(3)	output	
72	sa(2)	output	
73	sa(1)	output	
74	sa(0)	output	
75	x8042cs	bidir	
76	drq2	*	This pin becomes TDO when JTAGEN is high.

0 SOFTWARE BACKWARD COMPATIBILITY

The following changes are not 100% compatible with the Élan Rev A silicon.

Status Readback Register, Index B3H, bit 0

Prior to Élan Rev B., any write to the Status Readback Register cleared Index B3[0]. In the Rev B., additional bits in the register are used for new functions. This requires the software to do a Read Modify Write cycle and clear bit 0.

Version Register, Index 64H

The value read from the Version Register, Index 64H is different in the Élan Rev B part from the readings obtained in the Élan Rev A part, to indicate what version of Élan the device is.

Port B, bit 5 - IOCHCHK status

This bit was set in the Élan Rev A when in Local Bus or Internal CGA Modes. In the Élan Rev B Am386SC300 this bit is cleared in Local Bus and Internal CGA modes.

I/O Registers 3D8H and 3D9H

In the Élan Rev A these register were write only, and reading was destructive. In the Élan Rev B Am386SC300 these registers are Read/Write.

JTAG Software Compatibility

The original Élan design used a noncombined Bidirectional cell. The effects are that during a sample/preload test for every bidir pad cell an additional shift must be performed to load data in all the boundary cells. The total number of shifts required for Élan Rev A is 219, and for Élan Rev B it is 173. Two pins, 8042CS and SYSCLK, were changed from outputs in Rev A to bidirectional in Rev B.

0 REV.A. TO REV.B. PCB DESIGN COMPATIBILITY

RESIN# and IORESET#

The Élan Rev B has two reset inputs in order to support the new Micro Power mode. These two inputs are RESIN# and IORESET# (please refer to the Micro Power mode section for details regarding these two signals). If Micro Power mode is not to be used the system designer should simply short these two inputs together and drive both signals with the system power on reset source. Note that the RESIN# signal on the Elan Rev B is a 3.3 volt only input.

In order for an Élan Rev B device to function properly in an existing Rev A PCB design a slight modification is required. The RESIN# and IORESET# inputs should be shorted and driven by the system power on reset source. The system designer may wish to use a zero ohm resistor jumper arrangement on the board in order to accommodate either the Rev A device or the Rev B part. If the system Power-On-Reset source is 5V, it will have to be translated to 3.3V for the Rev B part. The RESIN# input is pin #141 on both Rev A and Rev B Élan. Pin #140 on Élan Rev A is the RESERVED pin and is required to be pulled down externally. Pin # 140 on Élan Rev B is the IORESET# input.

The RESIN# input of Élan Rev B is referenced to the VCC CORE power plane only. It is therefore a 3.3 volt only compatible input. The Élan Rev A board design will have to level translate the RESIN# signal to 3.3 volts. See the diagram below for the suggested jumper arrangement for a single board design to support both a Rev A or a Rev B part when the Micro Power mode is not to be used.

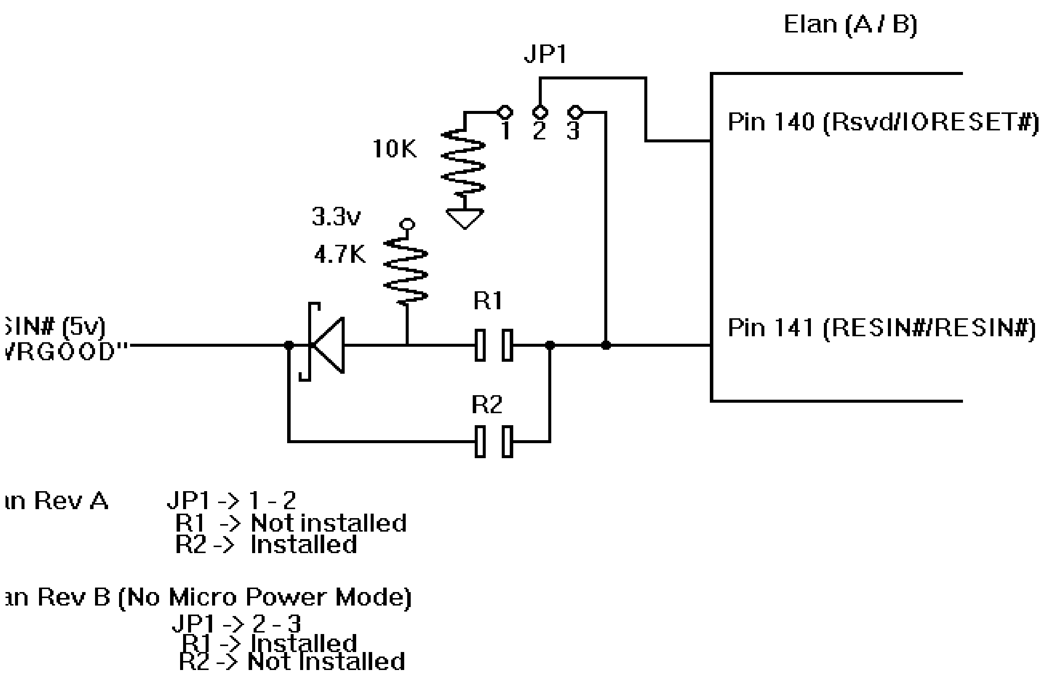


Figure 9. Jumper Arrangement, Micro Power Mode Not Used

16M bit DRAMs

The Élan Rev B part supports asymmetrically addressed 16M bit DRAMs (1M x 16 bit). The Élan Rev B pin# 60 is now the additional dram address signal MA11/SA12 to support these drams. Élan Rev A only supported dram address signals MA10 to MA0 shared with the SA23 to SA13 signals.

In Élan Rev A local bus mode, the upper local bus address signals A23 - A13 are not shared with the upper MA/SA signals. Instead, the upper local bus address signals are dedicated outputs. The remainder of the local bus address signals are shared with SA12 to SA0 for Élan Rev A. Since Élan Rev B has added an MA11 signal to be shared with SA12 a new local bus A12 signal has to be used so as not to share a DRAM address signal with a local bus address signal. Therefore, in the Élan Rev B the signal LVDD#/BALE (pin# 145) becomes local bus address signal A12 in local bus mode.

This Élan Rev B change only requires a Rev A PCB change if local bus mode is used. See the diagram below for the suggested jumper arrangement to for a single board design to support both a Rev A or a Rev B part in local bus mode.

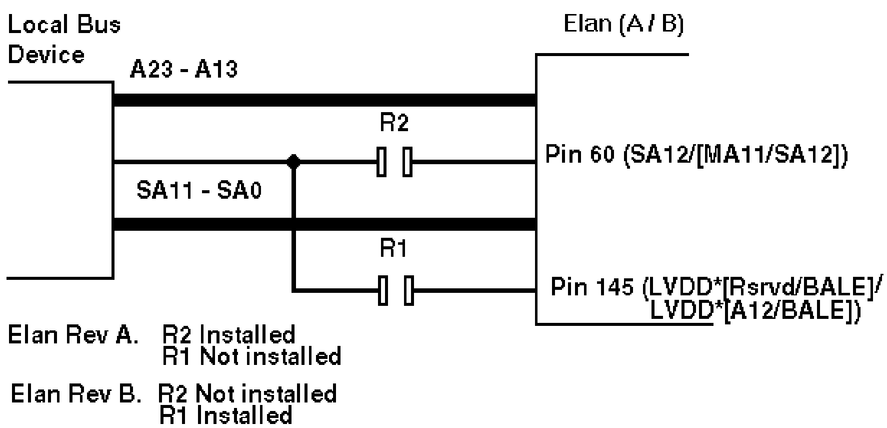


Figure 10. Jumper Arrangement, Local Bus Mode

Pin Characteristics

Some of the Élan Rev B Pin Characteristics have been changed from Élan Rev A. In terms of Rev A to Rev B PCB design compatibility, the only potential issues other than those already discussed are that some of the Clock Off mode pin states have specifically been changed in order to minimize system power in Clock Off modes such as Suspend. Please see the Rev B Pin Characteristics Table and all Rev A to Rev B changes which are highlighted in the following tables.

Memory Interface Pins

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State(volts) Internal CGA	Local BUS	Max. ISA	VCC IO	VCC Clamp	Spec. Load
RAS0# **(1)**	2	O		D	Active	3.3/0	3.3/0	3.3/0	VMEM	VMEM	50
RAS1# **(1)**	3	O		D	Active	3.3/0	3.3/0	3.3/0	VMEM	VMEM	50
CAS1L# [SRCS0#] **(1,2)**	4	O		D	Active	3.3/0	3.3/0	3.3/0	VMEM	VMEM	30
CAS1H# SRCS1#] **(1,2)**	5	O		D	Active	3.3/0	3.3/0	3.3/0	VMEM	VMEM	30
CAS0L# [SRCS2#] **(1,2)**	6	O		D	Active	3.3/0	3.3/0	3.3/0	VMEM	VMEM	30
CAS0H# [SRCS3#] **(1,2)**	7	O		D	Active	3.3/0	3.3/0	3.3/0	VMEM	VMEM	30
MA10 / SA13	10	O		E	0	3.3	3.3	3.3	VMEM	VMEM	70
MA9 / SA23	11	O		E	0	3.3	3.3	3.3	VMEM	VMEM	70
MA8 / SA22	13	O		E	0	3.3	3.3	3.3	VMEM	VMEM	70
MA7 / SA21	14	O		E	0	3.3	3.3	3.3	VMEM	VMEM	70
MA6 / SA20	15	O		E	0	3.3	3.3	3.3	VMEM	VMEM	70
MA5 / SA19	16	O		E	0	3.3	3.3	3.3	VMEM	VMEM	70
MA4 / SA18	17	O		E	0	3.3	3.3	3.3	VMEM	VMEM	70
MA3 / SA17	18	O		E	0	3.3	3.3	3.3	VMEM	VMEM	70
MA2 / SA16	19	O		E	0	3.3	3.3	3.3	VMEM	VMEM	70
MA1 / SA15	21	O		E	0	3.3	3.3	3.3	VMEM	VMEM	70
MA0 / SA14	24	O		E	0	3.3	3.3	3.3	VMEM	VMEM	70
MWE#	8	O		D	1	3.3	3.3	3.3	VMEM	VMEM	70
ROMCS#	44	O		B	1	5.0	5.0	5.0	VCC5	VSYS	30
DOSCS#	43	O		B	1	5.0	5.0	5.0	VCC5	VSYS	50

Notes: All inputs that have VCC Clamp = 5V are 5 volt safe inputs regardless of their VCC IO.

1. These signals are active during reset.
2. These pins always default to their DRAM interface function.

System Interface Pins

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State(volts) Internal CGA	Local BUS	Max. ISA	VCC IO	VCC Clamp	Spec. Load
MA11/SA12	60	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA11	61	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA10	62	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA9	63	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA8	64	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA7	66	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA6	67	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA5	69	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA4	70	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA3	71	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA2	72	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA1	73	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA0	74	O		D	0	0.0	0.0	0.0	VSYS	VCC5	70
D15	25	B	PD	D	0	0.0	0.0	0.0	VMEM	VMEM	70
D14	26	B	PD	D	0	0.0	0.0	0.0	VMEM	VMEM	70
D13	27	B	PD	D	0	0.0	0.0	0.0	VMEM	VMEM	70
D12	28	B	PD	D	0	0.0	0.0	0.0	VMEM	VMEM	70
D11	29	B	PD	D	0	0.0	0.0	0.0	VMEM	VMEM	70
D10	30	B	PD	D	0	0.0	0.0	0.0	VMEM	VMEM	70
D9	31	B	PD	D	0	0.0	0.0	0.0	VMEM	VMEM	70
D8	32	B	PD	D	0	0.0	0.0	0.0	VMEM	VMEM	70
D7	34	B	PD	D	0	0.0	0.0	0.0	VMEM	VMEM	70
D6	36	B	PD	D	0	0.0	0.0	0.0	VMEM	VMEM	70
D5	37	B	PD	D	0	0.0	0.0	0.0	VMEM	VMEM	70
D4	38	B	PD	D	0	0.0	0.0	0.0	VMEM	VMEM	70
D3	39	B	PD	D	0	0.0	0.0	0.0	VMEM	VMEM	70
D2	40	B	PD	D	0	0.0	0.0	0.0	VMEM	VMEM	70
D1	41	B	PD	D	0	0.0	3.3	0.0	VMEM	VMEM	70
D0	42	B	PD	D	0	0.0	3.3	0.0	VMEM	VMEM	70
SYSCLK [XTCLK] **(1)**	45	0(STI)		B	0 (-)	5.0/0	5.0/0	5.0/0	VSYS	VCC5	30
IRQ1	195	I	PU	-	-	4.4	4.4	4.4	VCC1	VCC5	
PIRQ1(PIRQ1/IRQ6)	193	I	PU	-(-/-)	-(-/-)	3.3	3.3	3.3	VCC1	VCC5	
PIRQ0(PIRQ0/IRQ3)	194	I	PU	-(-/-)	-(-/-)	3.3	3.3	3.3	VCC1	VCC5	
DACK2# [TCK]	46	O (I)		B	1	5.0	5.0	5.0	VSYS	VCC5	30
DRQ2 [TDO]	76	I (O)	PD	A	-	0.0	0.0	0.0	VSYS	VCC5	30
AEN [TDI]	47	O (I)		B	1	0.0	0.0	0.0	VSYS	VCC5	30
TC [TMS]	49	O (I)		B	0	0.0	0.0	0.0	VSYS	VCC5	30
ENDIRL	50	O		B	1	5.0	5.0	5.0	VSYS	VCC5	30
ENDIRH	51	O		B	1	5.0	5.0	5.0	VSYS	VCC5	30
DBUFOE#	59	O		B	1	5.0	5.0	5.0	VSYS	VCC5	30
IOR#	54	O		C	1	5.0	5.0	5.0	VSYS	VCC5	50
IOW#	55	O		C	1	5.0	5.0	5.0	VSYS	VCC5	50
MEMR#	56	O		C	1	5.0	5.0	5.0	VSYS	VCC5	50
MEMW#	57	O		C	1	5.0	5.0	5.0	VSYS	VCC5	50
RSTDRV	58	O		A	0	5.0	5.0	5.0	VSYS	VCC5	30
IOCHRDY	192	STI	PU	-	-	3.3	3.3	3.3	VCC1	VCC5	

Notes: All inputs that have VCC Clamp = 5V are 5 volt safe inputs regardless of their VCC IO.

1. Reset State SYSCLK frequency is 4.6 MHz.

Keyboard Interface Pins

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock off	Reset State(volts) Internal Max. CGA	Local BUS	ISA	VCC IO	VCC Clamp	Spec. Load
8042CS#[XTDAT]	75	O**(STI)**		B	1(-)	5.0	5.0	5.0	VSYS	VCC5	30
RC#	78	I	PU	-	-	5.0	5.0	5.0	VSYS	VCC5	
A20GATE	79	I	PU	-	-	5.0	5.0	5.0	VSYS	VCC5	

Notes: All inputs that have VCC Clamp = 5V are 5 volt safe inputs regardless of their VCC IO.

Parallel Port Interface Pins

Signal Name	Pin No	I/O Type	Term	Drive Type	Clock Off	Reset State(volts) Internal CGA	Local BUS	Max. ISA	VCC IO	VCC Clamp	Spec. Load
AFDT# [XTOUT] **(1)**	80	O		D	Last state	5.0	5.0	5.0	VCC5	Notes	100
INIT# [PCMCWE#]**(1)**	89	O		D	Last state	0.0	0.0	0.0	VCC5	VCC5	100
STRB# **(1)**	83	O		D	Last state	5.0	5.0	5.0	VCC5	VCC5	100
SLCTIN# [PCMCOE#](1)	84	O		D	Last state	5.0	5.0	5.0	VCC5	VCC5	100
ACK#	88	I		-	-	5.0	5.0	5.0	VCC5	VCC5	
BUSY **(2)**	85	I		-	-	5.0	5.0	5.0	VCC5	VCC5	
ERROR#	86	I		-	-	5.0	5.0	5.0	VCC5	VCC5	
PE	82	I		-	-	5.0	5.0	5.0	VCC5	VCC5	
SLCT	87	I		-	-	5.0	5.0	5.0	VCC5	VCC5	
PPDWE# [PPDCS#]	90	O		B	1(1)	5.0	5.0	5.0	VCC5	VCC5	30
PPOEN#	91	O		B	1(1)	0.0	0.0	0.0	VCC5	VCC5	30

Notes: All inputs that have VCC Clamp = 5V are 5 volt safe inputs regardless of their VCC IO.

1. These outputs function as open-drain outputs in normal parallel port mode, and function as CMOS drivers when the EPPEN configuration is set
2. The parallel port interface BUSY input must have an external pull-up if the parallel port is to be used in EPP mode. If this pull-up is not present, accesses to the parallel port in EPP mode will lock up the system.

RS-232 Interface Pins

Signal Name	Pin No	I/O Type	Term	Drive Type	Clock Off	Reset State(volts) II nternal CGA	Local BUS	Max. ISA	VCC IO	VCC Clamp	Spec.Load
DTR# **(1)**	92	O		A	Last state	0.0	5.0	0	VCC5	VCC5	50
RTS# **(1)**	93	O		A	Last state	0.0	0.0	5.0	VCC5	VCC5	50
SOUT**(1)**	94	O		A	Last state	0.0	0.0	5.0	VCC5	VCC5	50
CTS#	96	I	PU			5.0	5.0	5.0	VCC5	VCC5	
DCD#	98	I	PU			5.0	5.0	5.0	VCC5	VCC5	
DSR#	97	I	PU			5.0	5.0	5.0	VCC5	VCC5	
RIN#	100	I	PU			5.0	5.0	5.0	VCC5	VCC5	
SIN	99	I	PU			5.0	5.0	5.0	VCC5	VCC5	

Notes: All inputs that have VCC Clamp = 5V are 5 volt safe inputs regardless of their VCC IO.

1. These pins are terminated externally per bus option selection.

Power Management Control Pins

Signal Name	Pin No	I/O Type	Term	Drive Type	Clock Off	Reset State(volts) Internal CGA	Local BUS	Max. ISA	VCC IO	VCC Clamp	Spec. Load
ACIN	101	I	PD	-	-	0.0	0.0	0.0	VCC5	VCC5	
EXTSMI	102	I	PD	-	-	0.0	0.0	0.0	VCC5	VCC5	
SUS/RES	103	STI		-	-	5.0	5.0	5.0	VCC5	VCC5	
PMC4 **(1)**	184	O		B	Active	0.0	0.0	0.0	VCC1	VCC5	50
PMC3 **(1)**	185	O		B	Active	3.3	3.3	3.3	VCC1	VCC5	50
PMC2 **(1)**	77	O		B	Active	0.0	0.0	0.0	VSYS	VCC5	50
PMC1 **(1)**	138	O		B	Active	0.0	0.0	0.0	VCC5	VCC5	50
PMC0 **(1)**	137	O		B	Active	0.0	0.0	0.0	VCC5	VCC5	50
PGP3	186	O		B	Active	3.3	3.3	3.3	VCC	VCC5	50
PGP2	187	O		B	Active	3.3	3.3	3.3	VCC	VCC5	50
PGP1	188	B		B	Active	3.3	3.3	3.3	VCC	VCC5	50
PGP0	189	B		B	Active	0.0	0.0	0.0	VCC	VCC5	50
BL1#	106	STI		-	-	5.0	5.0	5.0	VCC5	VCC5	
BL2 #	107	STI		-	-	5.0	5.0	5.0	VCC5	VCC5	
BL3#	108	STI		-	-	5.0	5.0	5.0	VCC5	VCC5	
BL4#	109	STI		-	-	5.0	5.0	5.0	VCC5	VCC5	
LPH#	190	O		B	Active	0.0	0.0	0.0	VCC1	VCC5	50

Notes: All inputs that have VCC Clamp = 5V are 5 volt safe inputs regardless of their VCC IO.

1. PMC outputs: four Low (PMC0, PMC1, PMC2, PMC4), one High (PMC3), default state after reset. All five are programmable as either active High or Low after reset.

PCMCIA Interface Pins

Signal Name	Pin No	I/O Type	Term	Drive Type	Clock Off	Reset State(volts) Internal CGA	Local BUS	Max. ISA	VCC IO	VCC Clamp	Spec. Load
MCEL_A#	129	O		C	1	5.0	5.0	5.0	VCC5	VCC5	50
MCEH_A#	130	O		C	1	5.0	5.0	5.0	VCC5	VCC5	50
VPP_A	131	O		B	Active	0.0	0.0	0.0	VCC5	VCC5	50
REG_A#	132	O		B	0	5.0	5.0	5.0	VCC5	VCC5	50
RST_A (1)	133	O		B	Tri-state	0.0	0.0	0.0	VCC5	VCC5	50
CD_A#	110	STI		-	-	5.0	5.0	5.0	VCC5	VCC5	
RDY_A# (2)	111	I		-	-	0.0	0.0	0.0	VCC5	VCC5	
WP_A (2)	112	I		-	-	0.0	0.0	0.0	VCC5	VCC5	
BVD2_A (2)	113	STI		-	-	0.0	0.0	0.0	VCC5	VCC5	
BVD1_A (2)	114	STI		-	-	0.0	0.0	0.0	VCC5	VCC5	
WAIT_AB#(2)	115	I		-	-	5.0	5.0	5.0	VCC5	VCC5	
ICDIR	122	O		C	1	5.0	5.0	5.0	VCC5	VCC5	50
MCEL_B#	123	O		C	1	5.0	5.0	5.0	VCC5	VCC5	50
MCEH_B#	124	O		C	1	5.0	5.0	5.0	VCC5	VCC5	50
VPP_B	125	O		A	Active	0.0	0.0	0.0	VCC5	VCC5	50
REG_B#	126	O		A	0	5.0	5.0	5.0	VCC5	VCC5	50
RST_B (1)	127	O		B	Tri-state	0.0	0.0	0.0	VCC5	VCC5	50
CD_B#	116	STI		-	-	5.0	5.0	5.0	VCC5	VCC5	
RDY_B# (2)	117	I		-	-	0.0	0.0	0.0	VCC5	VCC5	
WP_B (2)	118	I		-	-	0.0	0.0	0.0	VCC5	VCC5	
BVD2_B (2)	119	STI		-	-	0.0	0.0	0.0	VCC5	VCC5	
BVD1_B (2)	120	STI		-	-	0.0	0.0	0.0	VCC5	VCC5	
CA24	134	O		B	0	0.0	0.0	0.0	VCC5	VCC5	50
CA25	136	O		B	0	0.0	0.0	0.0	VCC5	VCC5	50

Notes: All inputs that have VCC Clamp = 5V are 5 volt safe inputs regardless of their VCC IO.

1. External weak pull-down resistor required.
2. The reset state of these signals will be zero only if the reset state of the PCMCIA power source is zero. All of these pins are required to be pulled up to the PCMCIA power source externally.

Display Interface Pins

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State(volts) Internal CGA	Local BUS	Max. ISA	VCC IO	VCC Clamp	Spec. Load
DSMD7 (ADS# / 0WS#)	172	B (O/I)		C	0 (1/-)	0.0	3.3	3.3	VCC1	VCC5	50
DSMD6 (D/C# / DRQ0) (1)	171	B (O/I)		C	0 (LS/-)	0.0	3.3	0.0	VCC1	VCC5	50
DSMD5 (M/IO# / DRQ3) (1)	170	B (O/I)		C	0 (LS/-)	0.0	0.0	0.0	VCC1	VCC5	50
DSMD4 (W/R# / DRQ7) (1)	169	B (O/I)		C	0 (LS/-)	0.0	0.0	0.0	VCC1	VCC5	50
DSMD3 (BHE# / IRQ9) (1)	168	B (O/I)		C	0 (LS/-)	0.0	0.0	3.3	VCC1	VCC5	50
DSMD2 (BLE# / IRQ11) (1)	167	B (O/I)		C	0 (LS/-)	0.0	0.0	3.3	VCC1	VCC5	50
DSMD1 (LRDY# / DRQ6)	166	B (I/I)		C	0 (-/-)	0.0	0.0	0.0	VCC1	VCC5	50
DSMD0 (LDEV# / RSRVD)	148	B (I/O)		C	0 (-/-3-state)	0.0	3.3	0.0	VSYS2	VCC5	50
DSMA14 (A23 / LA23)	149	O		C	0	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA13 (A22 / LA22)	150	O		C	0	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA12 (A21 / LA21)	151	O		C	0	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA11 (A20 / LA20)	152	O		C	0	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA10 (A19 / LA19)	153	O		C	0	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA9 (A18 / LA18)	154	O		C	0	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA8 (A17 / LA17)	155	O		C	0	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA7 (A16 / DACK0#)	158	O		C	0 (0/1)	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA6 (A15 / DACK3#)	159	O		C	0 (0/1)	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA5 (A14 / DACK7#)	160	O		C	0 (0/1)	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA4 (A13 / DACK6#)	161	O		C	0 (0/1)	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA3 (CPUCLK/PULL UP) (2)	162	O		E	0	3.3	920/0	3.3	VCC1	VCC5	50
DSMA2 (CPURST/ RSRVD)	163	O		C	0	3.3	3.3	0.0	VCC1	VCC5	50
DSMA1 (NA# / IRQ7)	164	O (I/I)		C	0 (-/-)	3.3	3.3	3.3	VCC1	VCC5	50
DSMA0 (387RESET / PULLUP)	165	O(0/I)		C	0(0/-)	0.0	3.3	3.3	VCC1	VCC5	50
DSWE# (387ERR# / PULLUP)	183	O (I/I)		B	1 (-/-)	3.3	3.3	3.3	VCC1	VCC5	30
DSOE# (CPURDY# / LMEG#)	147	O		B	1	5.0	0.0	0.0	VSYS2	VCC5	50
DSCE# (DACK1# / DACK1#)	146	O		B	1	0.0	3.3	5.0	VSYS2	VCC5	30
LCDD0 [I] (DRQ1 / DRQ1)	174	O (I/I)		C	0 (-/-)	0.0	0.0	0.0	VCC1	VCC5	-
LCDD1 [R] (DACK5#/DACK5#)	144	O		C	0 (1/1)	3.3	3.3	5.0	VSYS2	VCC5	-
LCDD2 [G] (DRQ5 / DRQ5)	175	O (I/I)		C	0 (-/-)	0.0	3.3	0.0	VCC1	VCC5	-
LCDD3 [B] (IOCHCHK# / IOCHCHK#)	177	O (I/I)		C	0 (-/-)	0.0	3.3	3.3	VCC1	VCC5	-
M (IRQ4 / IRQ4)	173	O (I/I)		C	0 (-/-)	0.0	3.3	3.3	VCC1	VCC5	-
CP1 [HDRV] (PREQ / IRQ5)	178	O (I/I)		C	0 (-/-)	0.0	0.0	3.3	VCC1	VCC5	-
CP2 [VD0] (BUSY# / IRQ10)	179	O (I/I)		C	0 (-/-)	0.0	0.0	3.3	VCC1	VCC5	-
FRM [VDRV] (IRQ12 / IRQ12)	181	O (I/I)		C	0 (-/-)	0.0	3.3	3.3	VCC1	VCC5	-
LVEE# (IRQ15 / IRQ15)	182	O (I/I)		B	1 (-/-)	3.3	3.3	3.3	VCC1	VCC5	50
LVDD# (A12 / BALE)	145	O		XE	1(0/1)	3.3	3.3	5.0	VSYS2	VCC5	50
IOCS16# [LCDDL0]	196	I [B]		C	- [0]	3.3	3.3	3.3	VCC1	VCC5	70
MCS16# [LCDDL1]	197	I [B]		C	- [0]	3.3	3.3	3.3	VCC1	VCC5	70
IRQ14 [LCDDL2]	198	I [B]		C	- [0]	0.0	0.0	0.0	VCC1	VCC5	70
SBHE# [LCDDL3]	143	O[B]		C	0[0]	0.0	0.0	0.0	VSYS2	VCC5	70

Notes: All inputs that have VCC Clamp = 5V are 5 volt safe inputs regardless of their VCC IO.

1. LS in the Clock Off column stands for “Last State”.
2. In Local bus during reset this signal is 920-mV/0-V frequency = 32kHz

Miscellaneous Interface Pins

Signal Name	Pin No	I/O Type	Term	Drive Type	Clock Off	Reset State(volts) Internal Max. CGA	Local BUS	ISA	VCC IO	VCC Clamp	Spec Load
IORESET# (1)	140	I		-	-	0.0	0.0	0.0	VCC5	VCC5	
X32IN (2)	201	I		-	-	640mV	920/0	920/0	AVCC	AVCC	
X32OUT (3)	202	O		osc.	Active	168/0	168/0	168/0	AVCC	AVCC	-
LF1	204	A		-	-	1.52	1.52	1.52	AVCC	AVCC	
LF2	205	A		-	-	1.48	1.48	1.48	AVCC	AVCC	
LF3	206	A		-	-	1.52	1.52	1.52	AVCC	AVCC	
LF4	207	A		-	-	1.68	1.68	1.68	AVCC	AVCC	
X1OUT [BAUD_OUT]	200	O		B	0(lLast state)	0.0	1.24	1.24	VCC1	VCC5	-
RESIN#	141	STI		-	-	0.0	0.0	0.0	VCC	VCC	
SPKR (4)	139	O		B	LS	5.0	5.0	5.0	VCC5	VCC5	50
JTAGEN	199	I	PD	-	-	0.0	0.0	0.0	VCC1	VCC5	

Notes: All inputs that have VCC Clamp = 5V are 5 volt safe inputs regardless of their VCC IO.

1. This pin should be terminated via a 10k pull-down resistor if Micro Power mode is being used and this input is not driven by external logic at all times.
2. In Local bus and Max ISA bus configurations, during reset this signal is 920mV/0V frequency = 32kHz.
3. This signal is 1.68-V/0-V frequency = 32kHz.
4. "LS" in the Clock Off column stands for "Last State".

Power Pins

Signal Name	Pin No	I/O Type	Term	Drive Type	Clock Off	Reset State(volts) I Internal Max. CGA	Local BUS	ISA	VCC IO	VCC Clamp	Spec. Load
AVCC						3.3	3.3	3.3			
VCC						3.3	3.3	3.3			
VCC5						5.0	5.0	5.0			
VSYS2						3.3	3.3	5.0			
VSYS						5.0	5.0	5.0			
VMEM						3.3	3.3	3.3			
VCC1						3.3	3.3	3.3			

Notes: All inputs that have VCC Clamp = 5 V are 5 volt safe inputs regardless of their VCC IO.

0 REV.B. PCB DESIGN CONSIDERATIONS

PCMCIA Signals

The Élan Rev A used the ISA bus signals MEMR# and MEMW# for the PCMCIA OE# and WE# signals respectively. With this arrangement, external logic was required to generate a separate OE# and WE# for the PCMCIA interface in order to avoid memory conflicts between PCMCIA memory space and ISA memory space. This situation has been specifically addressed in the Élan Rev B part.

The Élan Rev B provides two separate signals that are dedicated to be PCMCIA OE# and WE# outputs. These new signals are called PCMCOE# and PCMCWE# and are shared with the parallel port signals SLCTIN# and INIT# respectively. When the separate PCMCIA command signals are enabled via firmware the ISA command signals MEMR# and MEMW# will be generated for all ISA memory space cycles except those that the PCMCIA CE# signals are active for. The PCMCOE# and PCMCWE# command signals will be dedicated to PCMCIA memory space cycles. The parallel port functionality of the SLCTIN# and INIT# pins is no longer available when the separate PCMCIA command signal feature is enabled. If the parallel port functionality is required, the external logic approach that is necessary with an Élan Rev A design will be required.

Clocks

The Élan Rev A limited the systems designer to utilizing either a 14.336MHz clock or the Baudout clock from the on board UART out of the X1OUT [BAUD_OUT] pin (pin# 200). The Élan Rev B design allows the system designer to utilize both of these clocks simultaneously. If enabled via firmware, the 14.336MHz (X1OUT) clock may be enabled to be output on the parallel port signal AFDT# (pin# 80). The BAUD_OUT signal can then be selected to be driven out on pin# 200.

If the parallel port functionality is required the simultaneous clock feature will not be available.

Combining DOSCS# and ROMCS# Space

The Élan Rev B device provides a linear DOSCS# address decode. In order for a system designer to implement an on board R.F.A. (Resident Flash Array) or R.R.A. (Resident ROM Array) and boot the system from that array it is required that the Élan DOSCS# and ROMCS# are externally ored together on the board. In addition, if the array is implemented as a X16 memory interface, an external address decode circuit is required to drive the MCS16# signal back to Élan for the ROMCS# accesses. The MCS16# driver is required to be open collector if other devices will also be driving the MCS16# signal back to Élan. The DOSCS# interface can be programmed to be X16 before the first access to this space via the boot rom firmware. For this space, the external MCS16# generation is not required.

Micro Power Mode

If the Élan Rev B Micro Power mode is to be used, all of the specified timing requirements must be satisfied as outlined earlier in this document. In addition, an external 10k ohm pull-down resistor should be connected to the IORESET# input. This is required while in Micro Power mode if that signal is not specifically driven low by the external circuitry. If this input is not driven low in Micro Power mode the pull-down is required such that the input does not float and potentially cause Élan to exit the mode randomly.